Industrial Embedded Systems
- Design for Harsh Environment -

Dr. Alexander Walsch
alexander.walsch@ge.com

Part V

WS 2011/12

Technical University Munich (TUM)

Agenda

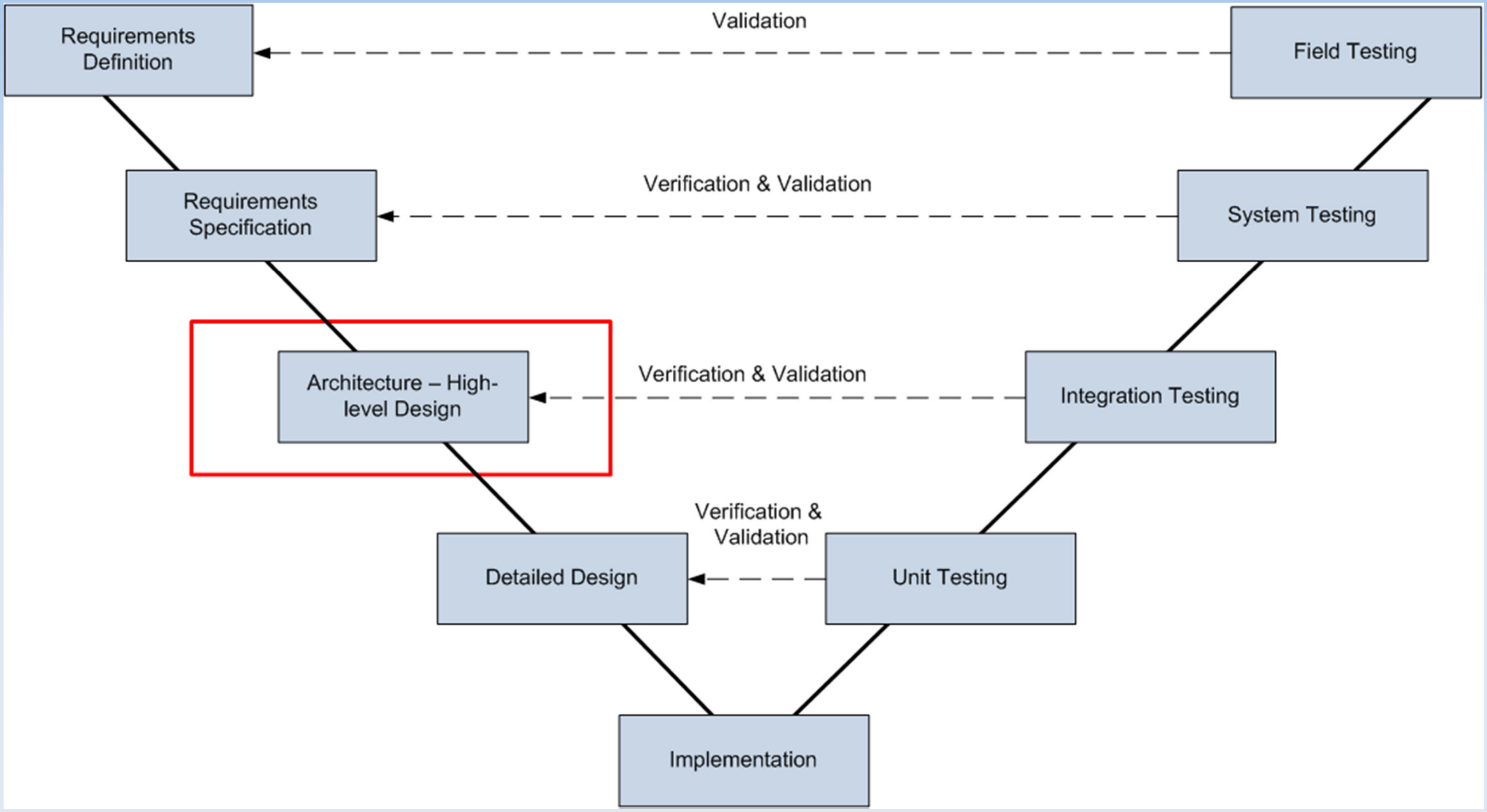
Today:

Architecture – High Level Design

Recap:

- Requirements Specification for PMU

V-Model


Requirements Definition
Validation
Field Testing
Requirements Specification
Verification & Validation
System Testing
Architecture – High-level Design
Verification & Validation
Integration Testing
Detailed Design
Verification & Validation
Unit Testing
Implementation

Overview

- We do have a requirements specification which describes the requirements at the system border at this point
- Define the major building blocks and their interfaces within the system:
  - Board, Connectors
  - Input, output, processing, power supply hardware
  - Input, output, scheduling, application software
- Define architecture constraints which are implied by safety and/or reliability requirements
- Describe how these blocks refer to the requirements in the requirements specification
- Compile an „architecture design document“

Approach

- Identify standards (coding, best practice, etc.) which should be used (overlap with requirements analysis)
- Define major system hardware components
- Specify major hardware building blocks and do rough a footprint calculation
- Identify hardware design patterns if applicable (reusable principles)
- Specify interfaces between hardware building blocks
- Specify major software building blocks and do rough a footprint calculation (e.g. OS, libraries)
- Identify software design patterns if applicable

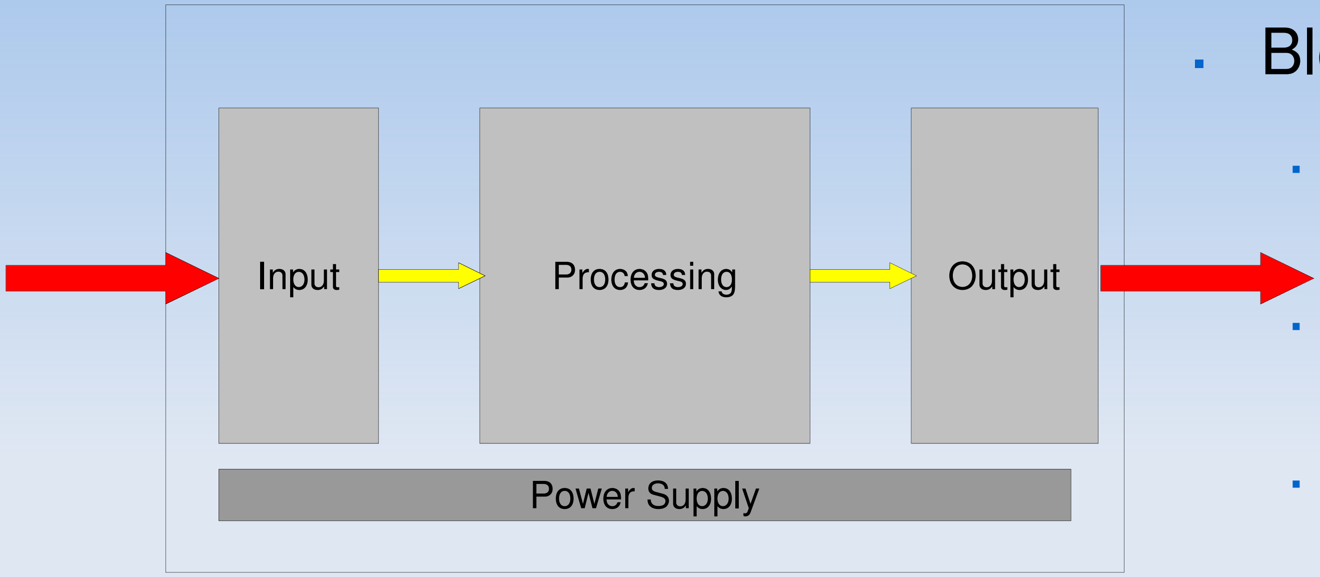
Standards and Best Practice

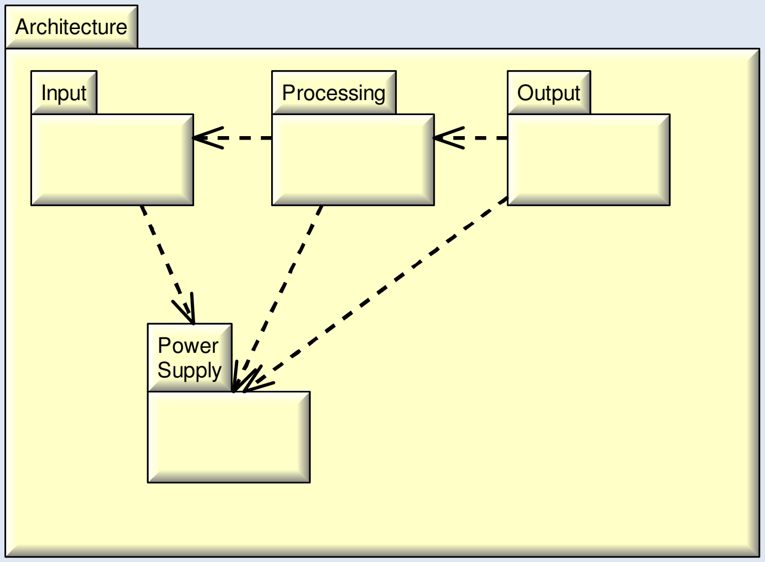
- Hardware
  - Company internal design practice: packages, traces, component size limits
  - Proven in use components (the latest stuff is not always the best)
  - Standards: architectural and design constraints imposed by certification
- Software
  - Company internal design practice
  - Coding standards (MISRA C/C++, JSF C++): what must be used and what is not permitted
  - Coding style guides: Look and feel of the SW code
  - Standards: architectural and design constraints imposed by certification

Standards and Best Practice Ctd.

- General
  - Ask more senior people who have gone through similar challenges in the past
  - Tools and their versions (HW CAD, CASE)
  - Aligned with the budget
  - Milestones and reviews

Graphical Representation





- Block diagram vs. UML:
  - Block diagram widely used in HW design
  - Easy to understand and sufficient for architectures
  - UML has no advantage since hardware needs to be described in CAD tool from scratch anyways

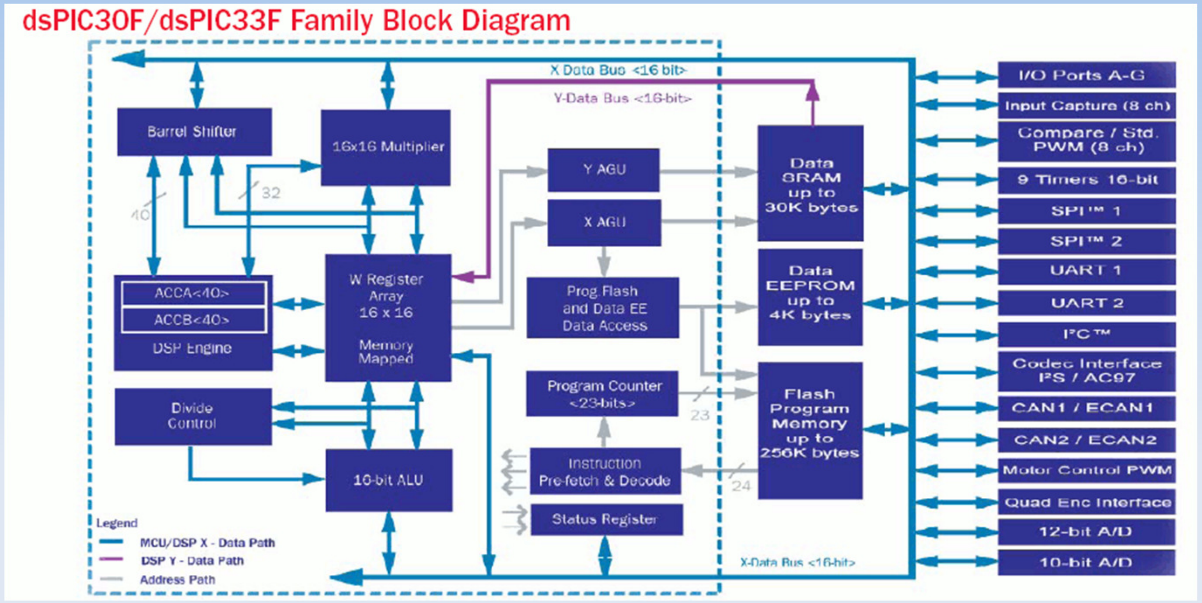
Major System Hardware Components

- We will look into the following components and introduce design patterns:
  - Processors - uC, DSP, general purpose
  - Reconfigurable electronics - CPLD, FPGA
  - Analog Input – Op Amps, INAs, filters, ADCs
  - Analog Outputs – DACs
  - Power supplies – step down/up converters
  - Boards
  - Connectors, Communication
- Afterwards we will try to take the patterns and apply it to the PMU

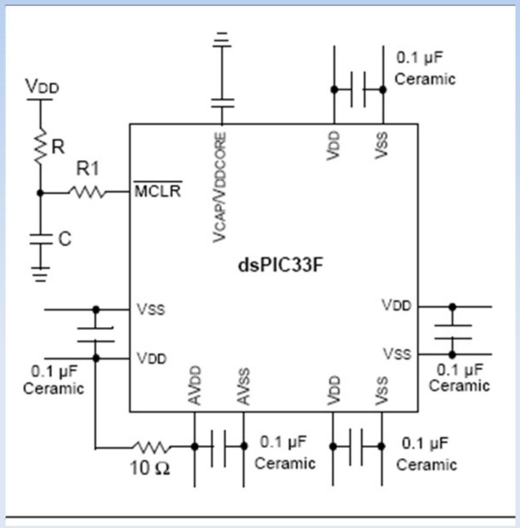
Processors

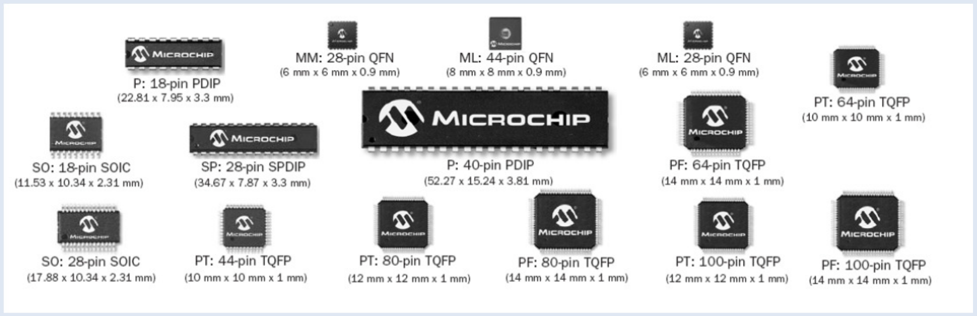
- Processor itself contains data path, control
- Embedded processors usually contain
  - Memory (SRAM, EEPROM, Flash)
  - Communication (UART, I2C, SPI, CAN, etc.)
  - Watchdog
  - Peripherals (ADC, DAC, PWM, Timer, Capture-Compare, etc.)
- Embedded processors are System-on-Chips and do not need any general hardware configuration. There are two add-ons that we want to highlight:
  - Reset circuitry (power on reset, brown out detection)
  - External watchdogs (program flow supervision)

Example: Microchip dsPIC



Source: microchip.com

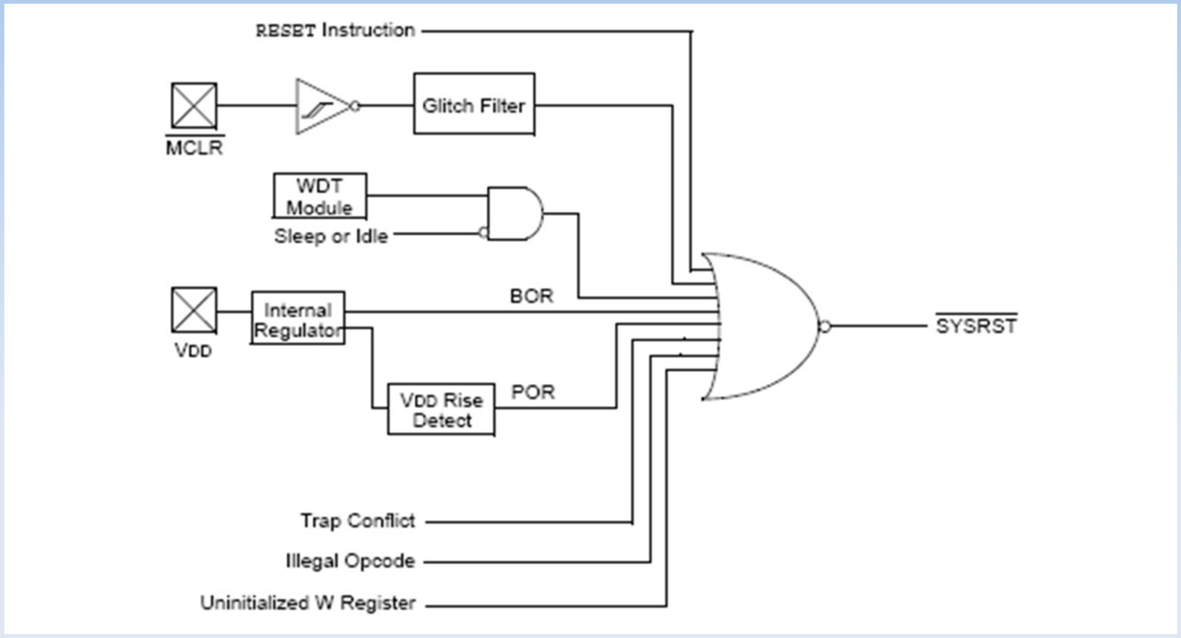



P: 18-pin PDIP (22.81 x 7.95 x 3.3 mm)
MM: 28-pin QFN (6 mm x 6 mm x 0.9 mm)
ML: 44-pin QFN (8 mm x 8 mm x 0.9 mm)
ML: 28-pin QFN (6 mm x 6 mm x 0.9 mm)
PT: 64-pin TQFP (10 mm x 10 mm x 1 mm)
SO: 18-pin SOIC (11.53 x 10.34 x 2.31 mm)
SP: 28-pin SPDIP (34.67 x 7.87 x 3.3 mm)
MICROCHIP
P: 40-pin PDIP (52.27 x 15.24 x 3.81 mm)
PF: 64-pin TQFP (14 mm x 14 mm x 1 mm)
SO: 28-pin SOIC (17.88 x 10.34 x 2.31 mm)
PT: 44-pin TQFP (10 mm x 10 mm x 1 mm)
PT: 80-pin TQFP (12 mm x 12 mm x 1 mm)
PF: 80-pin TQFP (14 mm x 14 mm x 1 mm)
PT: 100-pin TQFP (12 mm x 12 mm x 1 mm)
PF: 100-pin TQFP (14 mm x 14 mm x 1 mm)

Product	Pins	Flash Memory Kbytes	RAM Kbytes	DMA # Ch	Timer 16-bit	Input Capture	Output Compare/ Standard PWM	Codec Interface	A/D* 12-bit 500 ksps	UART	SPI™	I²C™	CAN	I/O Pins (max)†	Package Code
dsPIC33FJ64GP206	64	64	8	8	9	8	8	1	1 ADC, 18 Ch, 1 S/H	2	2	1	—	53	PT

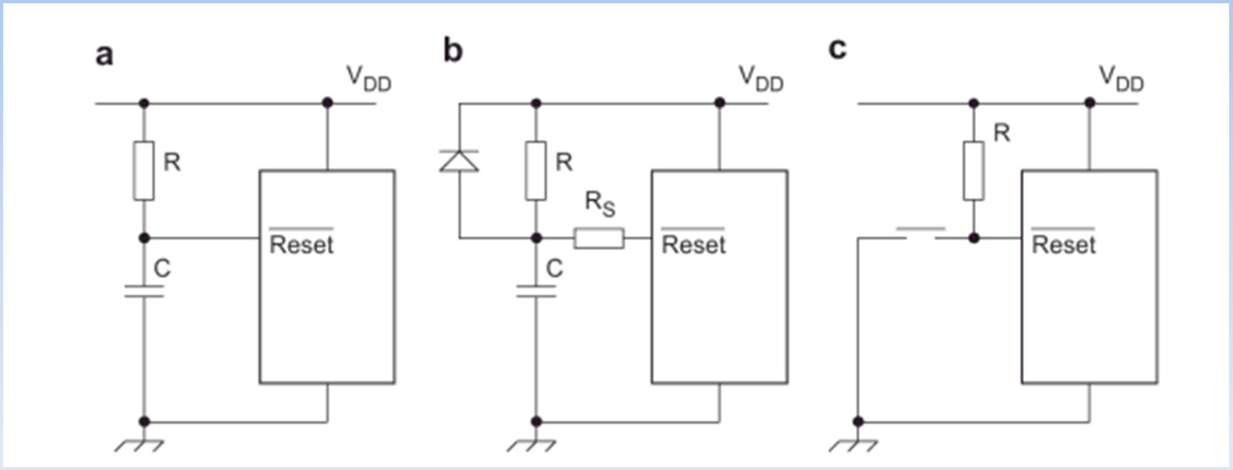
Reset Circuits

- Reset: puts the system into a defined state
- A reset can be requested for many reasons:
  - Instruction
  - External event or fault
  - Internal Fault
- The cause of a reset is usually indicated by a flag internal to the processor
- Reset stops the processor immediately. After release the reset vector is executed.



Source: microchip.com

Reset Circuits Ctd.
- Power on Reset -

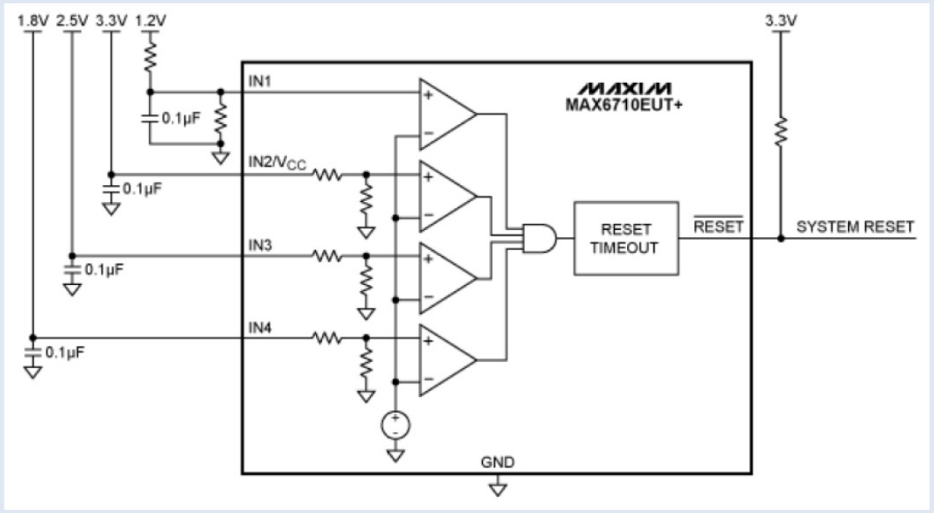


Source: Wilmshurst, Designing Embedded Systems with PIC Microcontrollers

- Example circuits for active low resets (processor is reset if voltage is low, operational if voltage is high)
  - a) simple power on reset circuit
  - b) reset pin current limitation, additional current path to allow quick power cycle with subsequent power on reset
  - c) reset button (only for lab tests – not populated in products)

Reset Circuits Ctd.
- Voltage Supervision -

- Commercial products require supervision of several board level voltages
- Voltage violations other than the processor voltage can cause erronous results
- Supervisory and reset circuits are available from all major IC companies (Maxim, Analog Devices, ...). There are programmable ones where limits can be set by software.

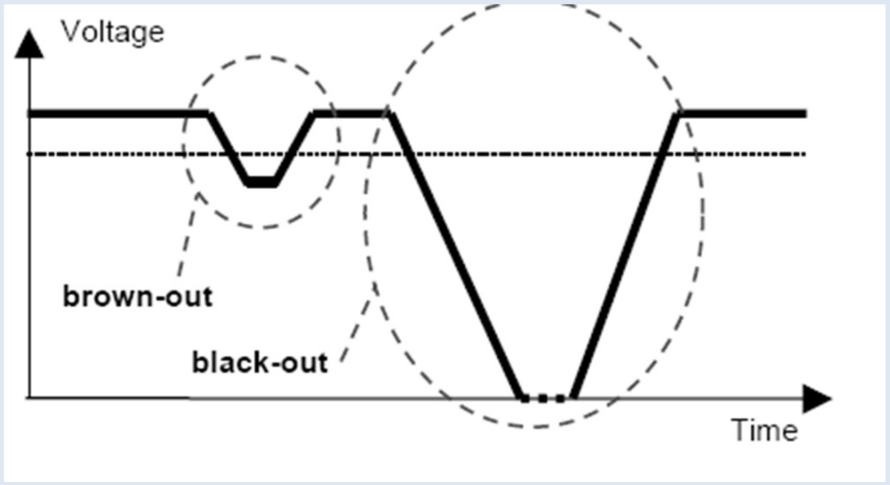


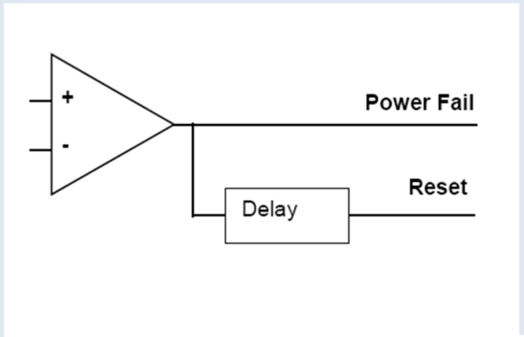
Source: Maxim AN540

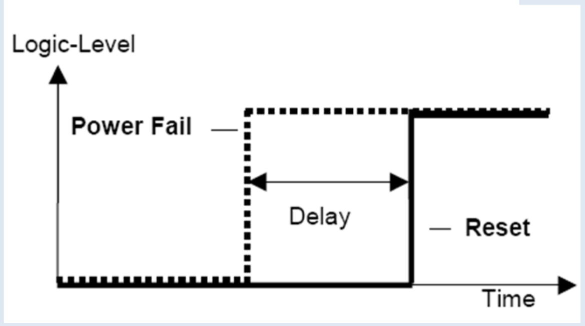
Reset Circuits Ctd.
- Brown Out Detection -

- Brown out detection (BOR) important for battery operated systems
- Voltage glitch or gradually decreasing voltage
- Some data might to be stored in non-volatile memory (e.g. EEPROM)
- Routing of a delayed reset to an NMI triggers a data storage routine

Source: Philips AN468



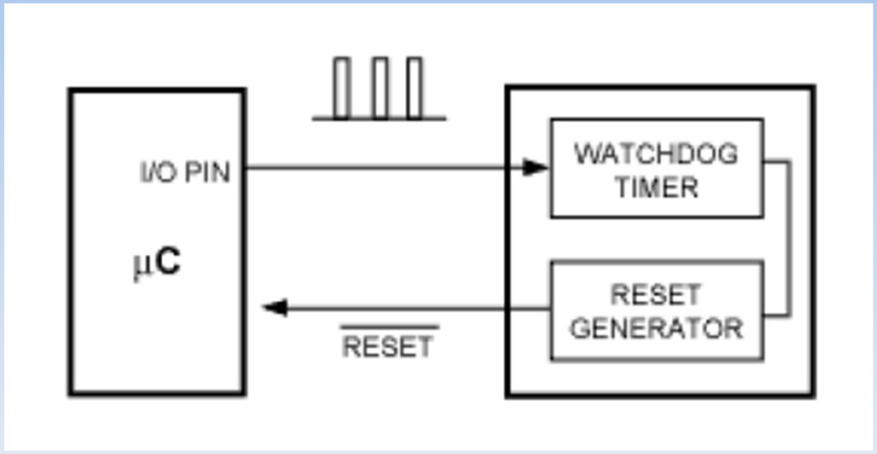


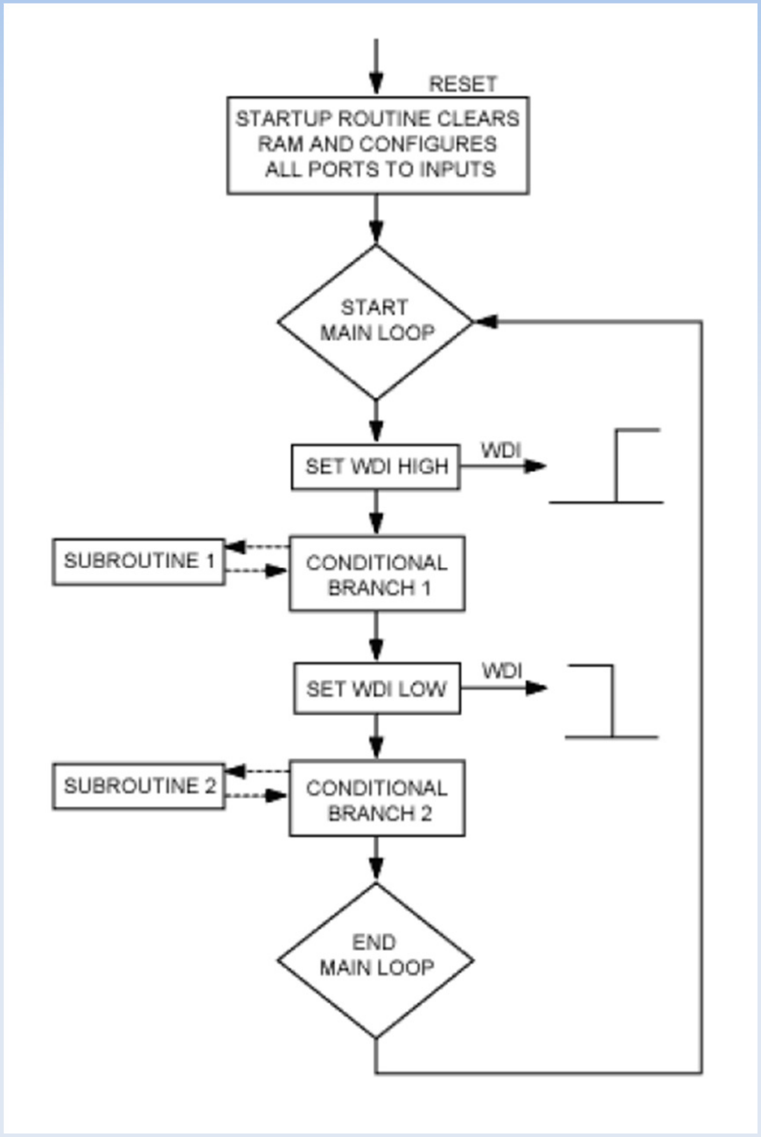


Watchdog Circuits

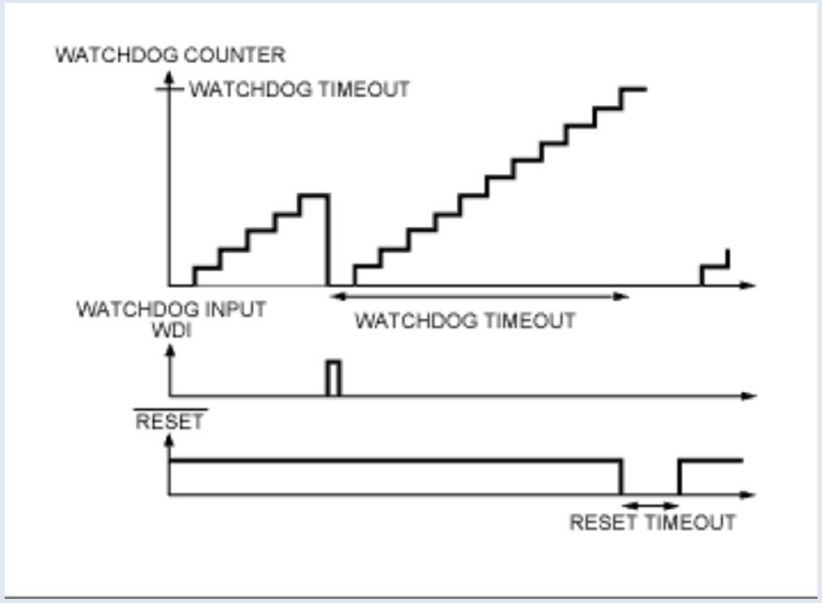
- A watchdog timer is a supervisory component which must be triggered in regular intervals in order to avoid system reset
- Embedded processors usually come with internal watchdog circuits.
- A possible failure mode of the oscillator (FMEA) makes a second external one with a separate clock source highly advisable for robust systems.
- Internal watchdogs can be disabled accidentally by software
- Set and reset the watchdog in different parts of the software to disallow stuck-at watchdog pulse loops

Watchdog Circuits Ctd.





Source:
Maxim AN1926

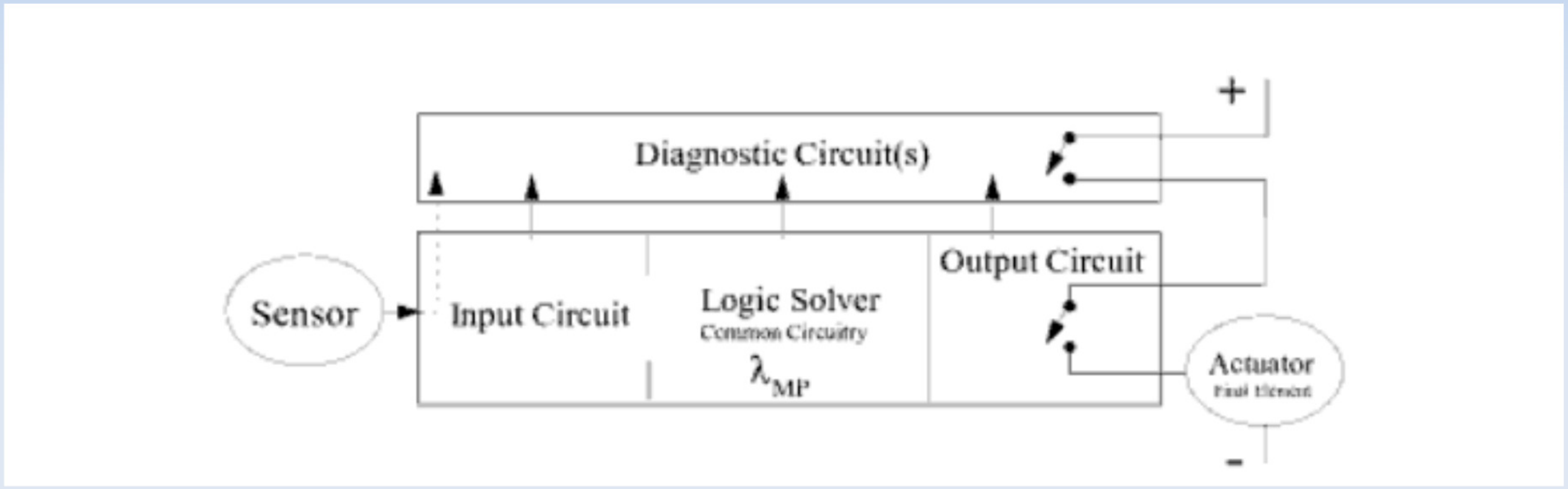


Watchdog Circuits Ctd.

- 1oo1D architecture: embedded processor is supervised by an external watchdog and a separate independent output is provided
- A single channel can fail dangerously and safely: λ_d, λ_s
- Dangeros failures (different failure modes) can be detected and undetected: λ_{dd}, λ_{du}
- Dangerous detected failures are „converted“ into safe failures (the response is the safe state).
- An external watchdog detects deviations in software execution sequence and timeliness and thus detects possible dangerous failures.
- Availability and safety aspects similar to results from lecture #4.

Watchdog Circuits Ctd.

- 1oo1D architecture:
  used when an independent way of de-energizing the output is used to achieve safety



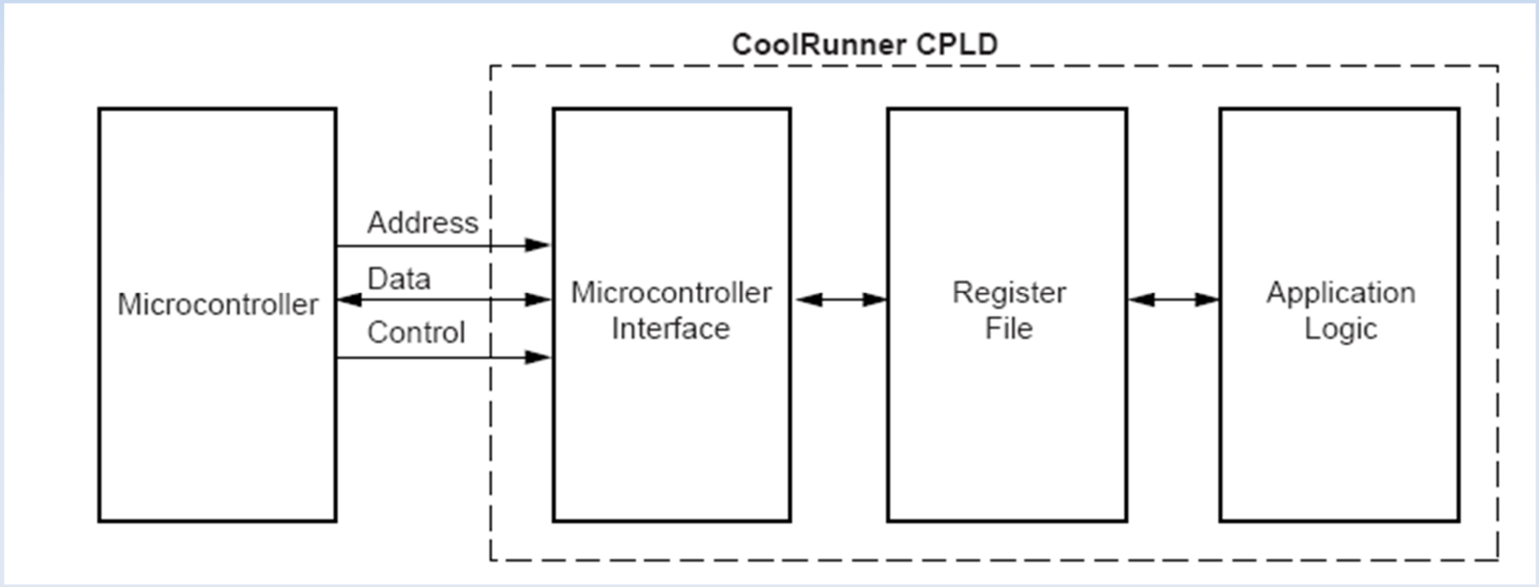
Source:
Goble, Control Systems
Safety and Reliability

Reconfigurable Electronics

- FPGAs, CPLDs widely used. More exotic reconfigurable components out there – e.g. analog FPAAs
- Functionality is specified by high-level languages (e.g. VHDL, Verilog) or schematic entry.
- Coprocessors for time-critical functions, I/O or signal processing. Connected via parallel or serial standard interface (digital) or configurable part of conditiong electronics.
- FPGAs mostly SRAM based (volatile) while CPLDs mostly Flash or EEPROM based (non-volatile).
- CPLDs are less complex and used for the realization of combinatorial and sequential electrical circuits with a deterministic pin-to-pin latency by design.
- FPGAs at the high end are very costly and hold complex circuitry.

Reconfigurable Electronics Ctd.

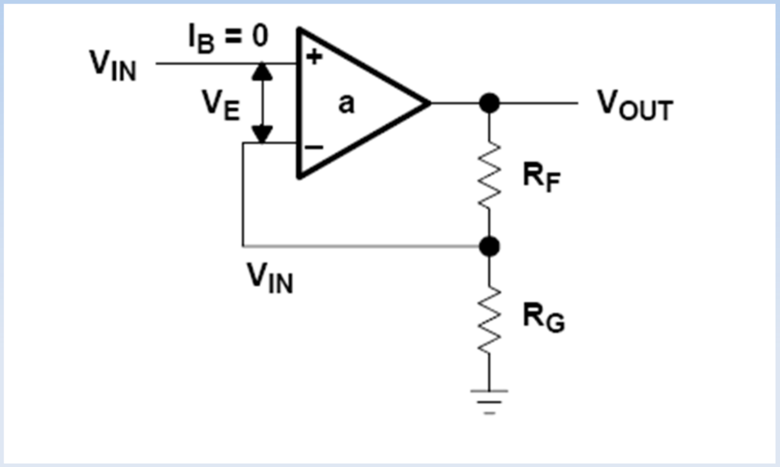
- FPGAs and CPLDs can be connected to embedded processors using either the system bus or a communication interface (SPI e.g.).



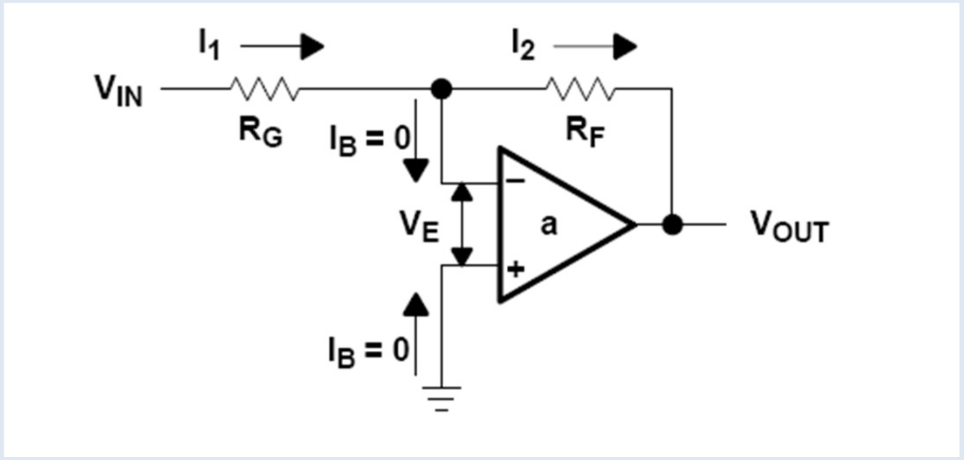
Source:
Xilinx XAPP349

Analog Electronics

- Non-inverting amplifier: $V_{out} = V_{in}\left(1 + \frac{R_F}{R_G}\right)$



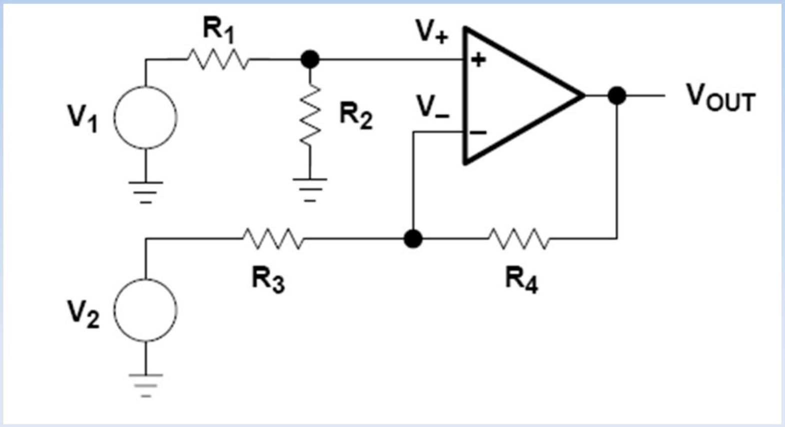
- Inverting amplifier: $V_{out} = -V_{in}\frac{R_F}{R_G}$



Source:
TI, Op Amps for Everyone

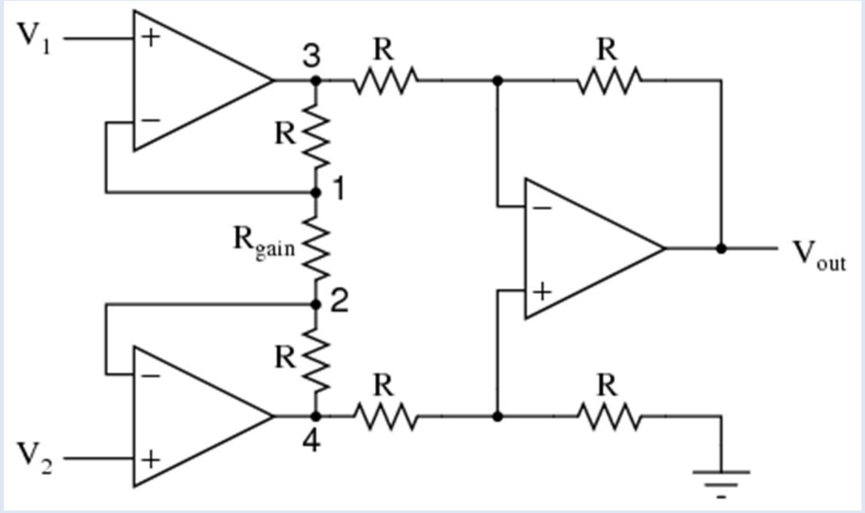
Analog Electronics Ctd.

- Differential amplifier: $V_{out} = (V_1 - V_2)\frac{R_4}{R_3}$



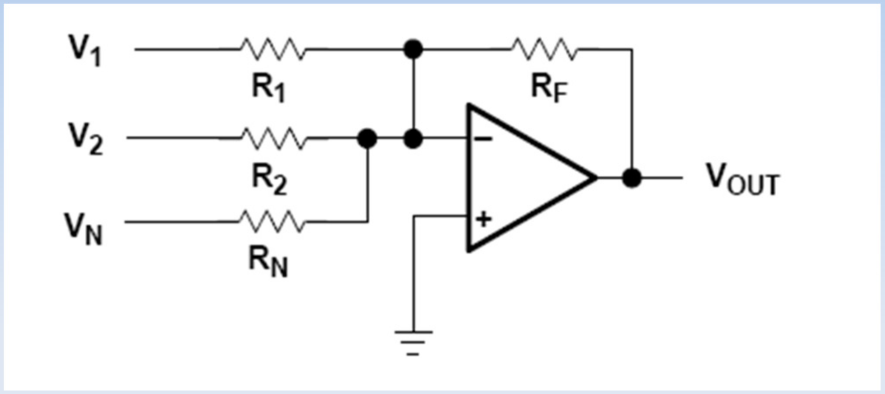
Source:
TI, Op Amps for Everyone

- Instrumentation amplifier: $V_{out} = (V_1 - V_2)\left(1 + \frac{2R}{R_{gain}}\right)$



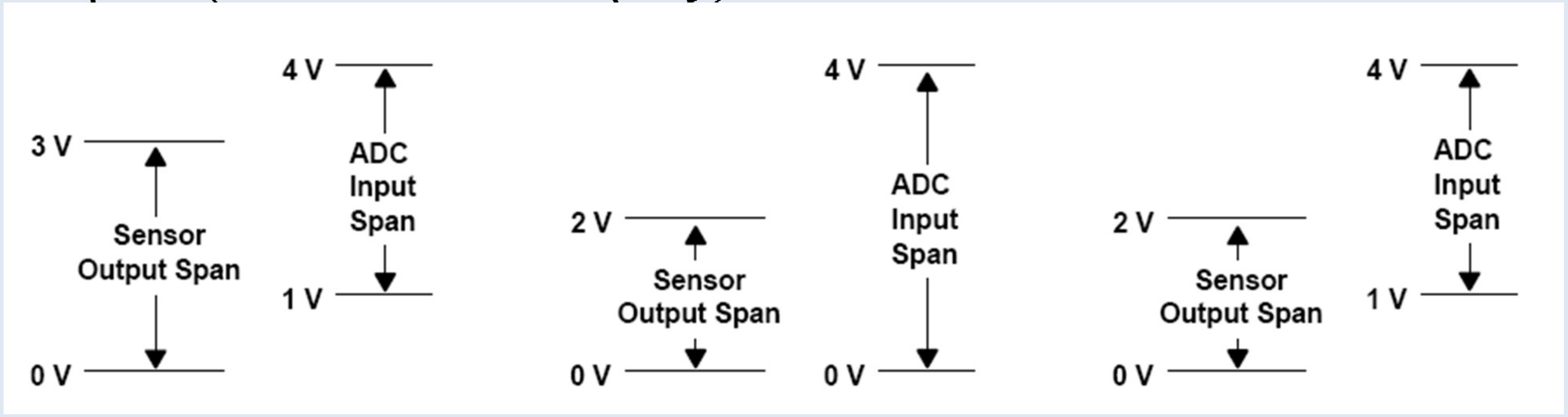
Analog Electronics Ctd.

- Adder: $V_{out} = -\left(\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_N}V_N\right)$



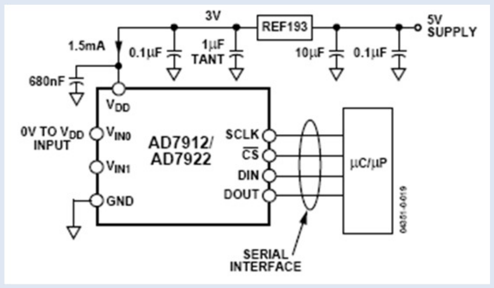
Source:
TI, Op Amps for Everyone

- What is that good for? - Adjust sensor output span to ADC input span (level shift + amplify):

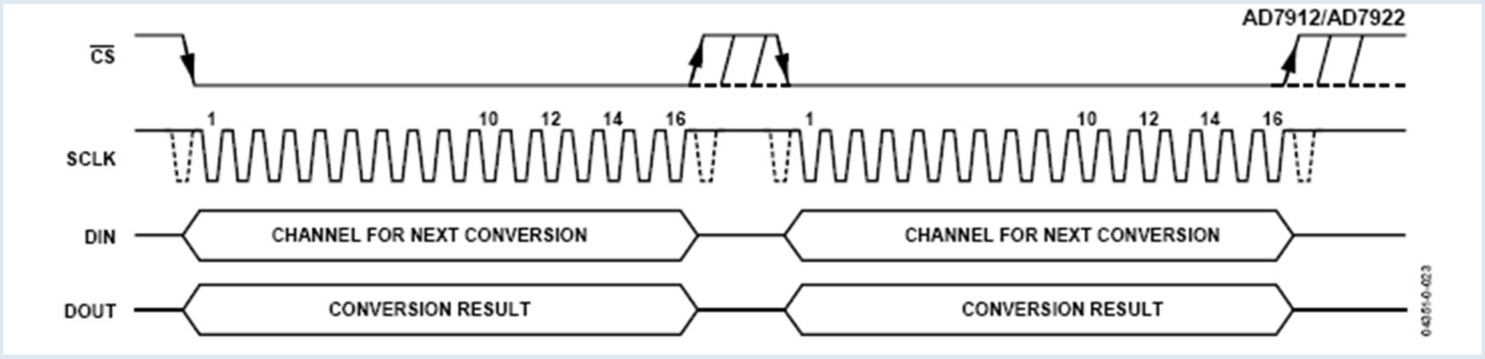


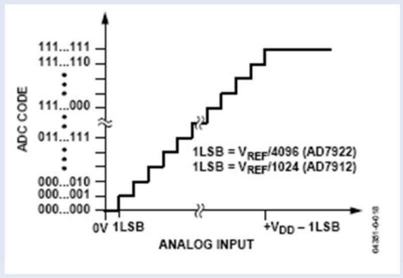
Mixed-signal Electronics - ADC -

- ADCs: analog to digital conversion
  - Internal to the embedded processor or external
  - Decision criteria (focus on low-bandwidth like monitoring):
    - Resolution: # of output bits (resolution of amplitude)
    - Sampling frequency (resolution in time)
    - #channels: e.g. 8 (e.g. sampling n channels simultaneously)
    - Input dynamic range: ratio between the largest and the smallest input
- Example: AD 7192



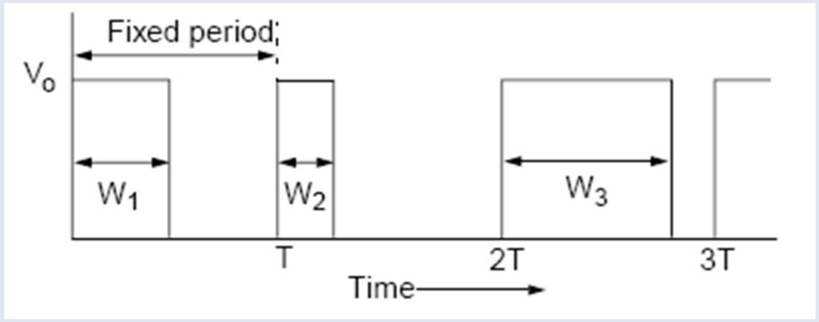
Source:
Analog Devices, AD7192





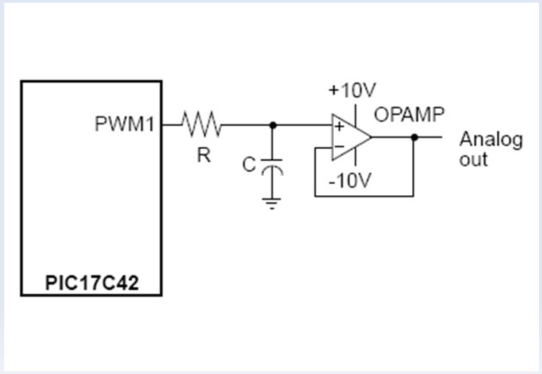
Mixed-signal Electronics - DAC -

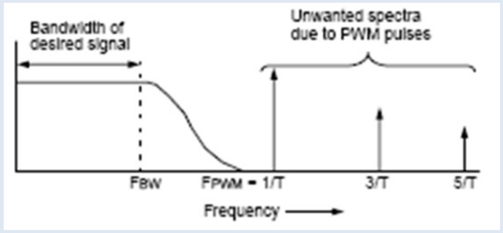
- DACs: digital to analog conversion
  - PWM, internal to embedded processor or external component
  - PWM:
    - Base frequency fixed, pulse width is a variable
    - Pulse width proportional to the amplitude of the unmodulated signal (a digital value provided to the PWM logic)



Source:
Microchip, AN538

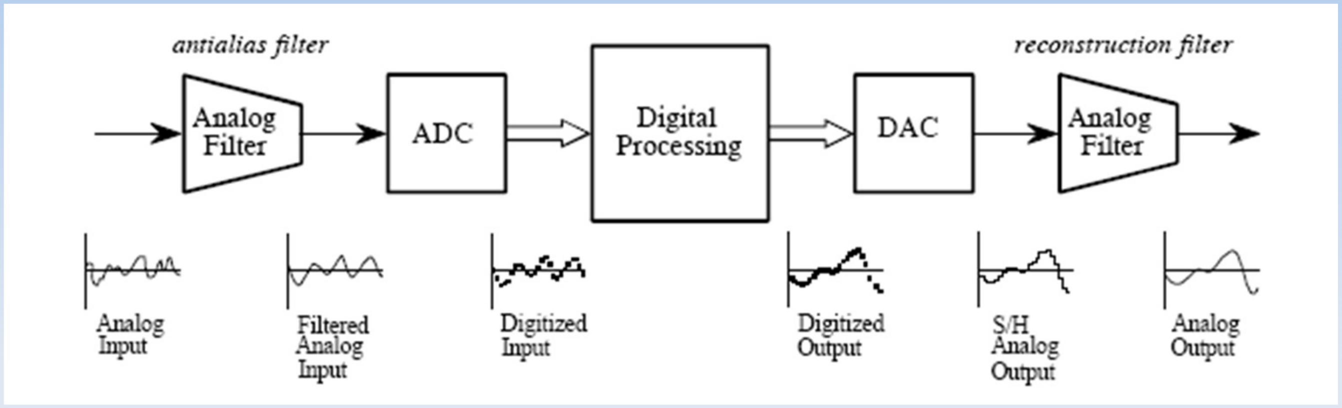
    - Use external low pass filter (RC) to extract analog information





Mixed-signal Electronics

- General signal chain:

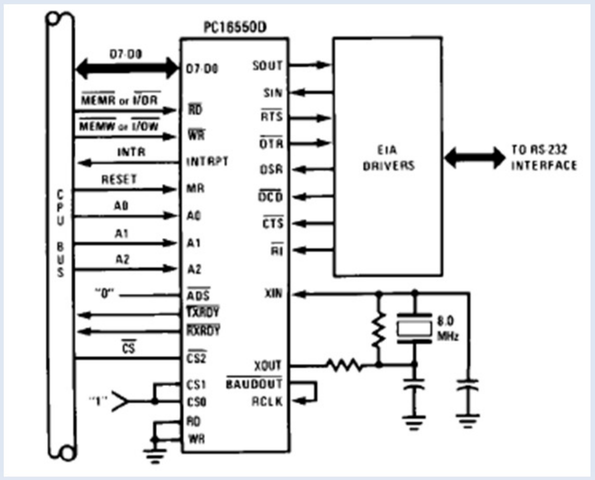


Source:
Smith, dspguide.com

- Analog filter: RC (simple), Sallen Key (more complex)
- ADC/DAC to processor interface: mostly standard serial for low bandwidth circuits (e.g. I2C, SPI) or integrated into embedded processor

Communication
- UART -

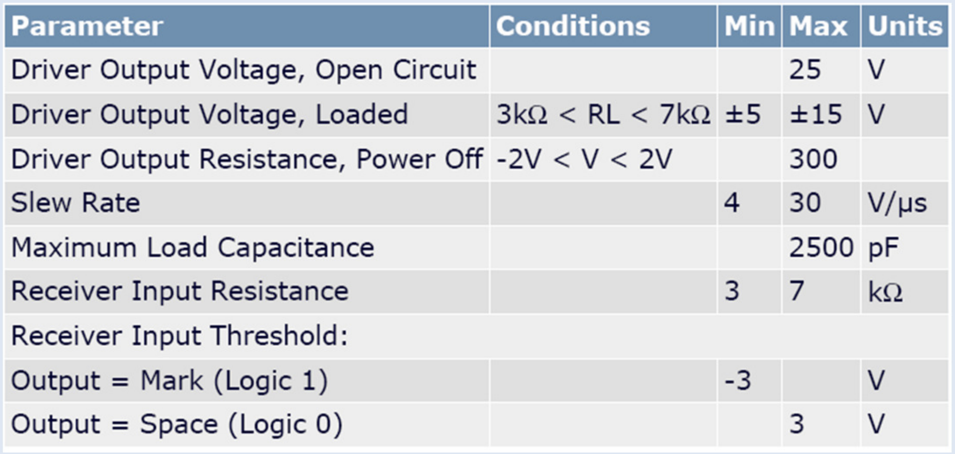
- UART: Universal Asynchronous Receiver/Transmitter
  - Literally any embedded processor comes with built in UART (sometimes we need more and need to connect an additional one)
  - Full-duplex asynchronous protocol which translates data from serial to parallel and vice versa
  - Defines start (synchronization), data, stop, parity bit(s) per frame
  - kbps to Mbps transmission rate, e.g. 9600baud
  - Physical link to other UARTs: TTL (native) , RS232 (single-ended), RS422/485 (differential) for off-board data transmission



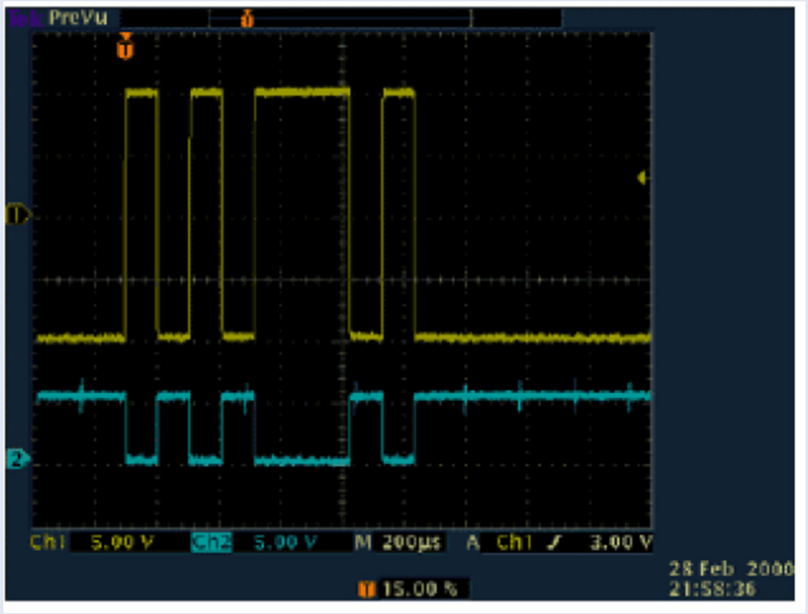
Source:
TI, PC16550D

Communication
- RS232 -

- Standard serial interface on older PCs. Now replaced by USB.
- Physical layer single-ended data transmission (usually point-to-point)
- Often used as debug interface in embedded systems, not used as regular data transmission line.
- e.g. MAX232 (Maxim), LTC2801 (LT)



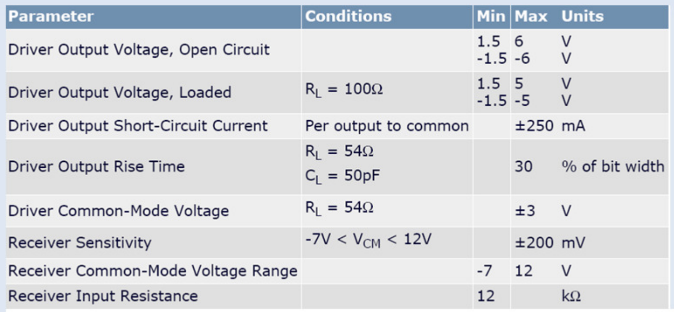
Parameter	Conditions	Min	Max	Units
Driver Output Voltage, Open Circuit			25	V
Driver Output Voltage, Loaded	3kΩ < RL < 7kΩ	±5	±15	V
Driver Output Resistance, Power Off	-2V < V < 2V		300	
Slew Rate		4	30	V/µs
Maximum Load Capacitance			2500	pF
Receiver Input Resistance		3	7	kΩ
Receiver Input Threshold:				
Output = Mark (Logic 1)		-3		V
Output = Space (Logic 0)			3	V



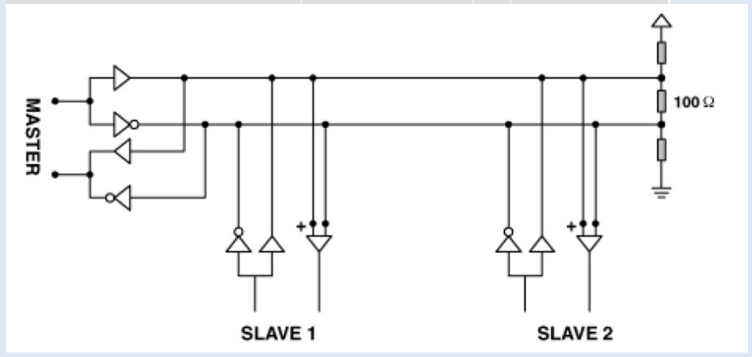
Source:
Maxim, AN723

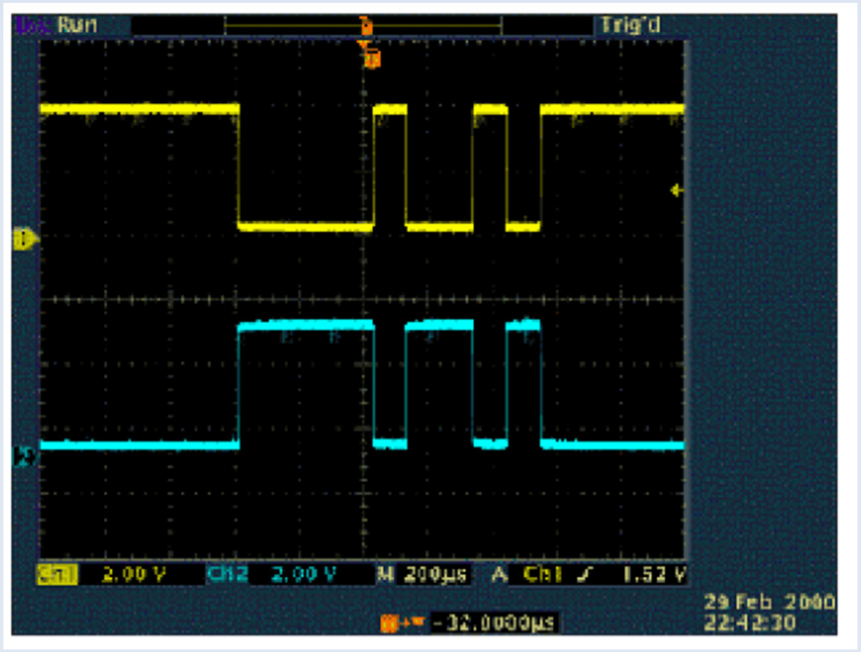
Communication
- RS422/485 -

- Physical layer differential data transmission (multi-drop)
- Often used as regular data transmission line since robust and inexpensive.
- RS422 and RS485 differ in increased common mode range and input impedance (RS485).



Parameter	Conditions	Min	Max	Units
Driver Output Voltage, Open Circuit		1.5 -1.5	6 -6	V V
Driver Output Voltage, Loaded	R_L = 100Ω	1.5 -1.5	5 -5	V V
Driver Output Short-Circuit Current	Per output to common		±250	mA
Driver Output Rise Time	R_L = 54Ω C_L = 50pF		30	% of bit width
Driver Common-Mode Voltage	R_L = 54Ω		±3	V
Receiver Sensitivity	-7V < V_{CM} < 12V		±200	mV
Receiver Common-Mode Voltage Range		-7	12	V
Receiver Input Resistance		12		kΩ

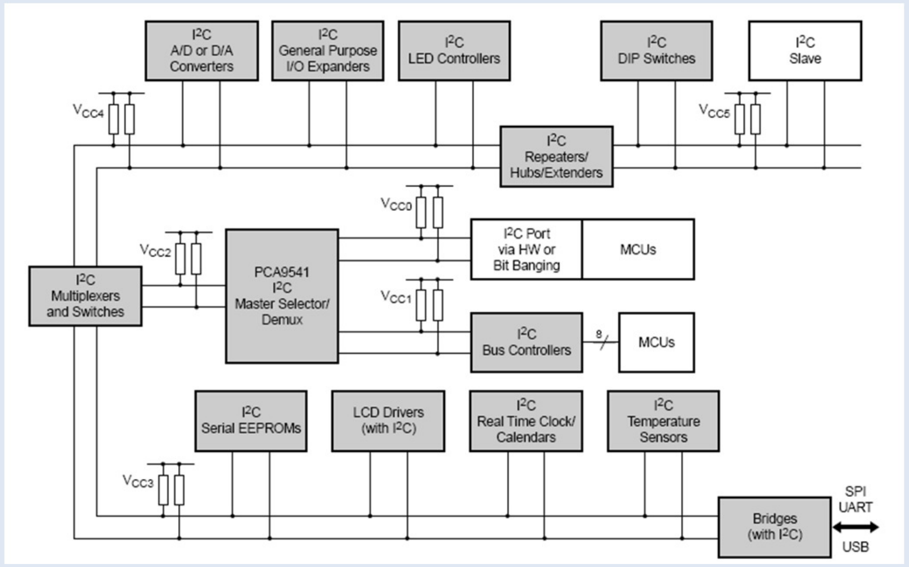




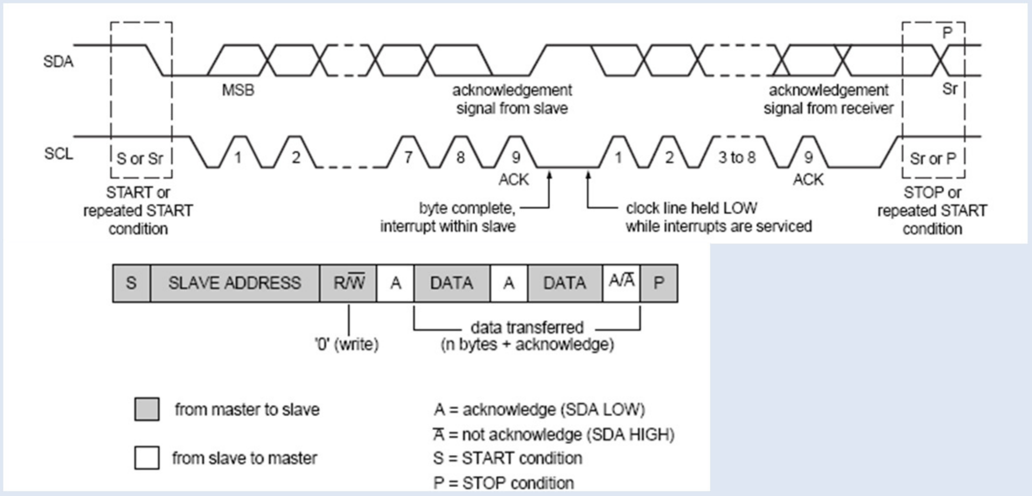
Source:
Maxim, AN723

Communication
- I2C -

- I2C: Inter-IC Bus, inexpensive, only two lines (SDA, SCL), master usually in embedded processor
- Each device is addressable by software
- Master/slave protocol, serial 8-bit oriented, multi-master bus, 100kbit/s in standard mode
- Protocols for additional low-speed peripheral connection



I²C A/D or D/A Converters
I²C General Purpose I/O Expanders
I²C LED Controllers
I²C DIP Switches
I²C Slave
V_CC4
V_CC5
I²C Repeaters/ Hubs/Extenders
V_CC0
V_CC2
PCA9541 I²C Master Selector/ Demux
I²C Port via HW or Bit Banging
MCUs
I²C Multiplexers and Switches
V_CC1
I²C Bus Controllers
8
MCUs
I²C Serial EEPROMs
LCD Drivers (with I²C)
I²C Real Time Clock/ Calendars
I²C Temperature Sensors
V_CC3
Bridges (with I²C)
SPI
UART
USB

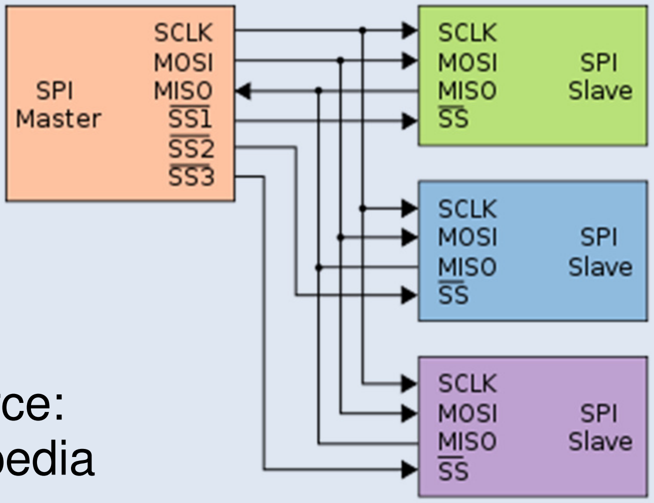


SDA
SCL
P
MSB
acknowledgement signal from slave
acknowledgement signal from receiver
Sr
S or Sr
1
2
7
8
9
ACK
1
2
3 to 8
9
ACK
Sr or P
START or repeated START condition
byte complete, interrupt within slave
clock line held LOW while interrupts are serviced
STOP or repeated START condition
S
SLAVE ADDRESS
R/W̄
A
DATA
A
DATA
A/Ā
P
'0' (write)
data transferred (n bytes + acknowledge)
from master to slave
from slave to master
A = acknowledge (SDA LOW)
Ā = not acknowledge (SDA HIGH)
S = START condition
P = STOP condition

Source:
NXP, UM10204

Communication
- SPI -

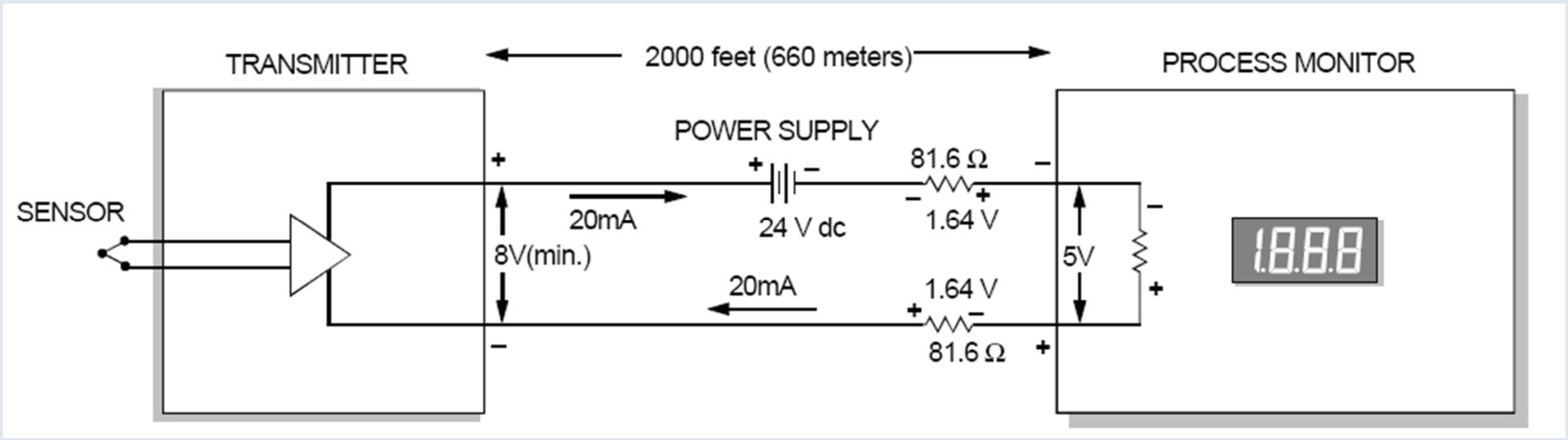
- SPI: Serial Peripheral Interface, common peripheral in embedded processors
- Used to move streams of data, bit rates in the MHz range
- Synchronous, master-slave
- Protocol for high-speed devices (Ethernet, ADC/DAC, …)
- As data is clocked out, new data is clocked in (data exchange)
- Clock (SCLK), Slave Select (SS)
- Master-out-slave-in (MOSI)
- Master-in-slave-out (MISO)



Source: wikipedia

Communication
- Current Loop -

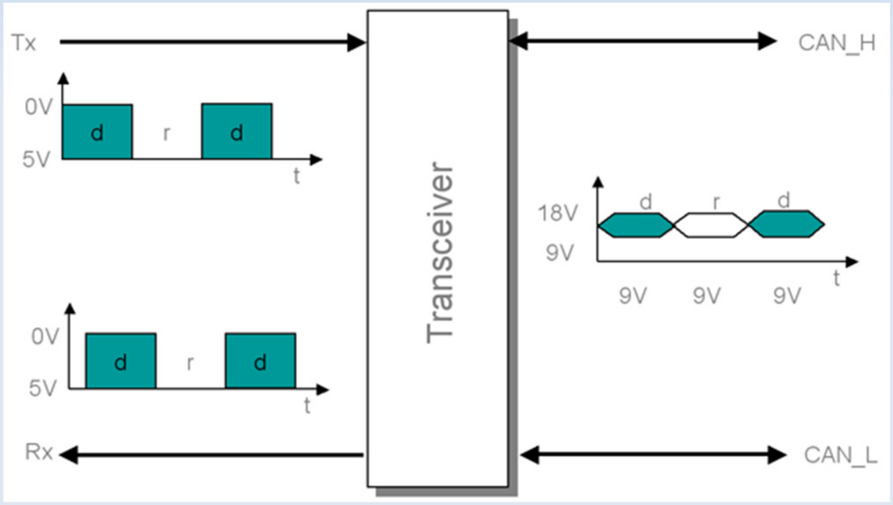
- 4-20 mA interface
  - Robust interface for sensor data transmission .
  - A sensor transmitter converts its reading into a current (4 mA being the zero level and 20 mA the FS of the sensor e.g.) - DAC
  - A receiver converts the current into a voltage for further usage - OpAmp
  - Advantage: loop voltage drops (line resistance) can be compensated, less sensitive to noise



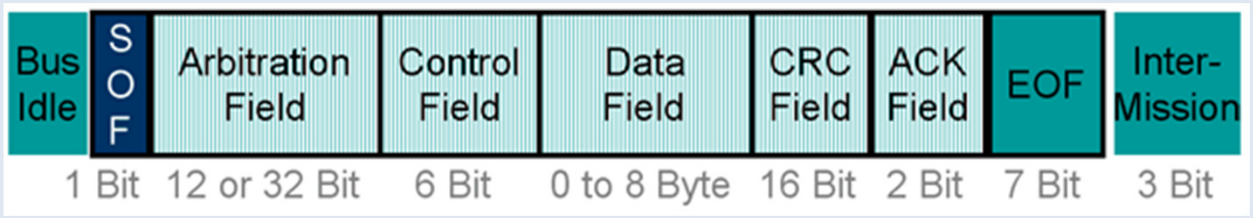
Source: Murata, DMS-AN-20

Communication
- CAN -

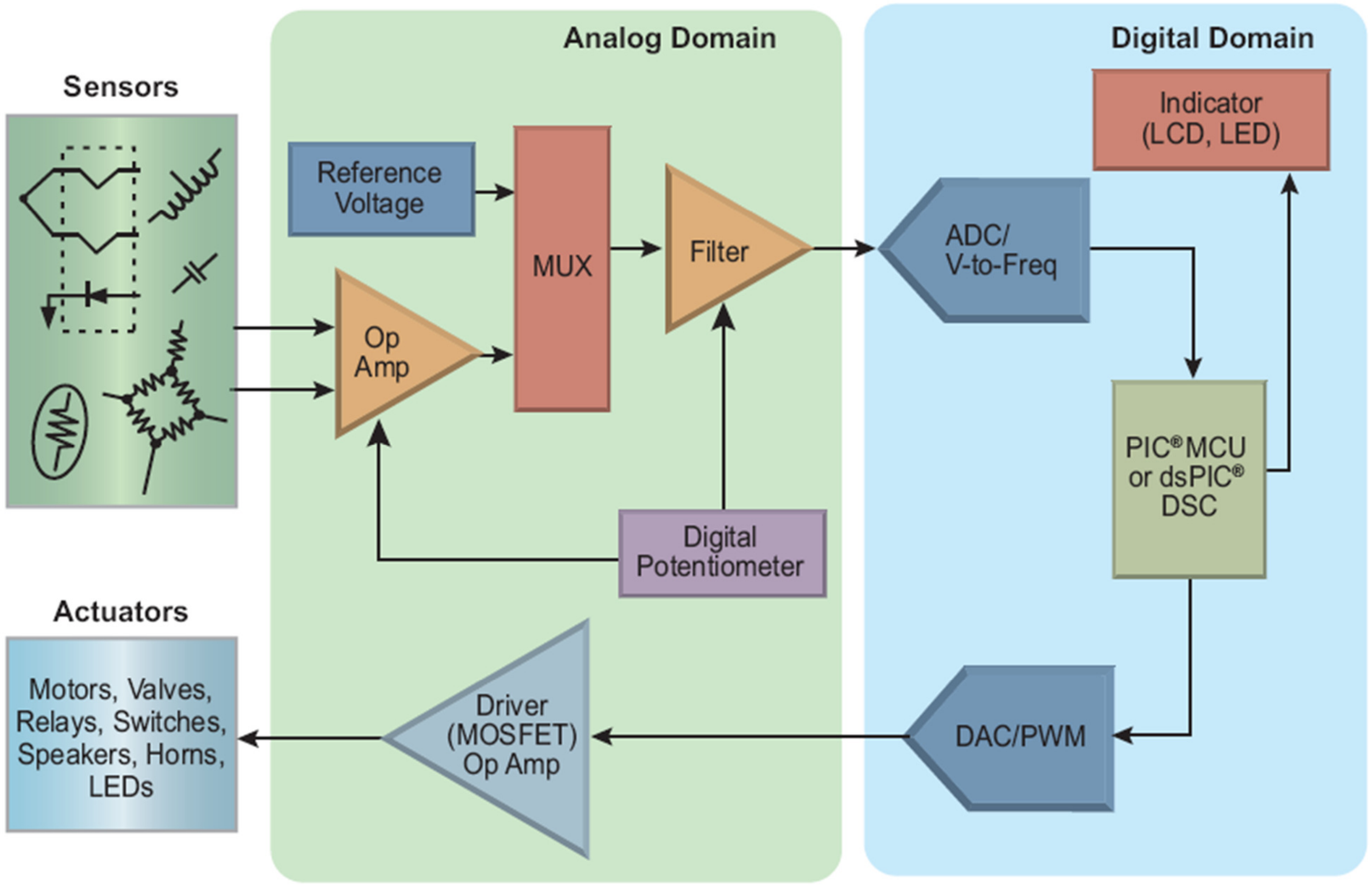
- CAN: Controller Area Network, ISO 11898 (PHY, DLL)
- Protocol controller available as peripheral of embedded processors, line driver external (creates differential signals, adds protection circuits)
- Serial protocol, up to 1 Mbit/s
- Bit-wise arbitration
- Error detection



Source:
Softing



Control Loop (from Microchip)


Analog Domain
Digital Domain
Sensors
Reference Voltage
MUX
Filter
Op Amp
Digital Potentiometer
ADC/ V-to-Freq
Indicator (LCD, LED)
PIC® MCU or dsPIC® DSC
DAC/PWM
Driver (MOSFET) Op Amp
Actuators
Motors, Valves, Relays, Switches, Speakers, Horns, LEDs